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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/163,925	09/30/1998	CHRISTIAN D. KASPER	98-C-020(520	6051

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EXAMINER

NGUYEN, PHUONGCHAU BA

ART UNIT

PAPER NUMBER

2665

DATE MAILED: 04/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/163,925

Applicant(s)

KASPER, CHRISTIAN D.

Examiner

Phuongchau Ba Nguyen

Art Unit

2665

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 9-30-1998 Application.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-42 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 33 recites the limitation "said HDLC ports" in line 3. There is insufficient antecedent basis for this limitation in the claim. Likewise, claim 36 recites "the HDLC port" in line 3.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-8,9-17,10-25,27-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Abiven (6,195,720).

**Regarding claim(s) 38:**

Abiven (6,195,720) discloses a network controller (fig.4) having:

a plurality of ports (422-425, 408-410, 412), each port including a FIFO receive memory (408-410, 412) for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields (;

a direct memory access unit (Adapter PCI 405, 414) for transferring a burst of data from the FIFO receive memory (408-410, 412) to an external system memory (system memory 401, 417) jointly shared with a host (processor 403, 419); and

a communications processor (control component 411; col.11, lines 36-39 wherein it selects the memory in write and read mode) for selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor (403, 419).

The preselected address field is inherent in the data packet transmitting via PCI bus, PCI adapter, bridge from one system to another as destination portion of the data packet, because with the preselected address field (i.e. destination) the data packet is not transmitted to anywhere in the network system as taught by Abiven.

**Regarding claim(s) 32:**

Abiven (6,195,720) discloses a system (fig.4) for routing network-based data arranged in frames comprising:

a host processor (403, 419) for analyzing transferred bursts of data and initiating an address and lookup algorithm for dispatching a frame to a desired destination;

a shared memory (401, 417) for receiving data, including any preselected address fields; and

a network device (405-406, 408-415, 420-425) having:

- a plurality of ports (422-425, 408-410, 412), each port including a FIFO receive memory (408-410, 412), for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;
- a direct memory access unit (405, 414) for transferring a burst of data from the receive memory to the shared system memory; and
- a communications processor (411) for selecting the amount of data to be transferred from the receive memory based on the desired address fields to be analyzed by the host processor.

The preselected address field is inherent in the data packet transmitting via PCI bus, PCI adapter, bridge from one system to another as destination portion of the data packet, because with the preselected address field (i.e. destination) the data packet is not transmitted to anywhere in the network system as taught by Abiven.

**Regarding claim(s) 37:**

A system according to Claim 32, wherein said receive memory comprises a first-in/first-out (FIFO) receive memory (408-410, 412; col.10, lines 58-63).

**Regarding claim(s) 27:**

Abiven (6,195,720) discloses a system (fig.4) for routing network-based data arranged in frames comprising:

a FIFO receive memory (408-410, 412) of a network device (405-406, 408-415, 420-425) for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a host processor (403, 419);

a shared system memory (401, 417) that exists between the network device and host processor for receiving data, including the preselected address fields, from the FIFO receive memory;

a direct memory access unit (405, 414) for transferring a burst of data from the FIFO receive memory to the shared system memory; and

a communications processor (411) for selecting the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address fields to be analyzed by the host processor.

The preselected address field is inherent in the data packet transmitting via PCI bus, PCI adapter, bridge from one system to another as destination portion of the data packet, because with the preselected address field (i.e. destination) the data packet is not transmitted to anywhere in the network system as taught by Abiven.

**Regarding claim(s) 28, 33, 39:** Abiven further discloses an interrupt bus (local bus 420-421) connected between the FIFO receive memory (i.e., 408, 412) and communications processor 411, wherein said ports include an interrupt generator {inherent in dual port memories 408, 412; col.11, lines 4-8, 39-40 wherein the interrupt

signal is generated from dual port memories 408, 412} for generating an interrupt to the communications processor along the bus.

**Regarding claim(s) 29, 34, 40:**

Abiven further discloses a FIFO bus (first PCI bus 404) connected between the direct memory access unit 405 and the FIFO receive memory (i.e., 409-410) on which data is transferred from the FIFO receive memory and through the direct memory access unit to a shared system memory 401.

**Regarding claim(s) 30, 35, 41:**

Abiven further discloses a controller bus (local bus 420-421) connected between the communications processor 411 and the direct memory access unit 405, 414 through which data transfer commands (col.13, lines 1-4 & 19-22) are issued from the communications processor to the direct memory access unit to transfer data.

**Regarding claim(s) 31, 36, 42:**

Abiven (6,195,720) does not explicitly disclose that said receive memory has a watermark setting at which the port issues a start-of-packet interrupt to the communications processor. The watermark is inherent in the memories {col.18, lines 11-21 wherein memories (i.e. 409) outputs signals such as "FIFO empty", "FIFO full", and possibly "FIFO half full" to control component 411 to stop the writing into memory when it is full and to stop reading from this memory when it is empty}.

**Regarding claim(s) 10:**

Abiven (5,691,985) disclose a method of controlling network data flow arranged in frames comprising the steps of:

receiving at least a first portion of a frame containing data receive memory (408-410, 412) of a network device (405-406, 408-415, 420-425), wherein the first portion of the received frame includes data having preselected address fields;

transferring a burst of data (by adapter PCI 405, 414), including preselected address fields, from the FIFO receive memory (408-410, 412) to a shared system memory (401 or 417) that exists between a host processor (403 or 419) and the network device; and

generating an interrupt signal (by dual port memories 408, 412) to the host processor (403 or 419) indicative that the preselected address fields of the frame are present in the memory {col.13, lines 19-24}.

**Regarding claim(s) 1, 19:**

Abiven (5,691,985) disclose a method of routing network-based data arranged in frames comprising the steps of:

receiving a first portion of a frame within a FIFO receive memory (408-410, 412) of a network device (405-406, 408-415, 420-425), wherein the first portion of the received frame includes data having preselected address fields;



Art Unit: 2665

transferring a burst of data (by adapter PCI 405, 414), including preselected address fields, from the FIFO receive memory (408-410, 412) to an external shared system memory (401 or 417) that exists between the network device and a host processor;

generating an interrupt signal (by dual port memories 408, 412) to the host processor (403 or 419) indicative that the preselected address fields of the frame are present in the shared system memory {col.13, lines 19-24}; and

initiating within the host processor (i.e. 403) an address and look-up algorithm in address tables (bistable 407) to determine frame routing based on the preselected address fields {col.12, lines 12-18 & 66-67; col.13, lines 4-24}.

**Regarding claim(s) 2, 11, 20:**

Abiven further discloses the step of transferring data from the receive memory through a direct memory access unit (adapter PCI 405, 414; col.13, lines 50-58).

**Regarding claim(s) 3, 12, 21:**

Abiven further discloses the step of generating an interrupt signal ( by dual port memories 408, 412) to the host processor (403, 419) from the receive memory (408-410, 412) after the direct access memory unit (adapter PCI 405, 414) has transferred data to the shared system memory (401, 419) {col.13, lines 14-58}.

**Regarding claim(s) 4, 13:**

Abiven further discloses the step of selecting the amount of data to be transferred {col.17, lines 65-68} from the receive memory based on the desired address fields to be analyzed by the host processor {col.17, line 50 to col.18, line 3}.

**Regarding claim(s) 5, 14, 22:**

Abiven further discloses the step of receiving the balance of the frame completely within shared system memory {col.18, lines 11-21 wherein the component control 411 stop writing when the memory is full and stop reading when the memory is empty}.

**Regarding claim(s) 6, 15, 23:**

Abiven further discloses the step of generating an end-of-frame interrupt (interrupt signal—to stop reading, when memory 409 is empty) when a frame has been completely received within shared system memory (401, 419){col.18, lines 11-21}.

**Regarding claim(s) 7, 16, 24:**

Abiven further discloses the step of generating a start-of-packet interrupt (interrupt signal—to stop writing, when memory 409 is full) to a communications processor 411 when the data received within the receive memory has reached a desired watermark value (memory is full){col.18, lines 11-21}.

Art Unit: 2665

**Regarding claim(s) 8, 17, 25:**

Abiven further discloses the step of issuing a command (to read or write) to a direct memory access unit of the network device to transfer data from the receive memory to the shared system memory after the communications processor has received the start-of-packet interrupt {col.13, lines 1-24; col.18, lines 13-15 & 59-60}.

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 9, 18, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abiven (6,195,720) in view of Lorenz (5,691,985).

Abiven (6,195,720) does not explicitly disclose the step of arbitrating use of a system bus between the direct memory access unit and a bus arbitration unit.

Lorenz (5,691,985) discloses a packet switch 47 comprising a packet bus 61 which includes an arbitration control 71 {col.4, lines 19-26}. Therefore, it would have been obvious to a skilled artisan to connect the arbiter 71 as taught by Lorenz to the PCI bus (404, 416) in Abiven's system and the motivation being to maintain orderly transmission access to the units by determining which unit has the right to transmit packets {Lorenz, col.4, lines 19-26}.

Art Unit: 2665

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuongchau Ba Nguyen whose telephone number is 703-305-0093. The examiner can normally be reached on Monday-Friday from 10:00 a.m. to 3:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 703-308-6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.



Phuongchau Ba Nguyen  
Examiner  
Art Unit 2665

April 22, 2002



HUY D. VU  
PRIMARY EXAMINER